Design and Characterization of High Performance 60 GHz Pseudomorphic MODFET LNAs in CPW-Technology Based on Accurate S-Parameter and Noise Models

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Abstract—**An accurate database for active and passive MMIC components valid up to millimeter-wave frequencies has been established. The CAE models for the transistors and the passive CPW-components, which include the coplanar T-junction, are derived from on-wafer S-parameter measurements up to 63 GHz. For noise modeling of the MODFETs up to millimeter-wave frequencies, we have pursued a novel approach which is based on the temperature noise model reported by Pospiezalski [1]. The parameter T_d which is required for the temperature model, is extracted from on-wafer noise parameter measurements up to 18 Ghz. Using this database, we have designed and fabricated low noise V-band 2-stage amplifiers using pseudomorphic MODFETs on GaAs substrate which have a performance of 10.5 dB gain and 5.2 dB noise figure at 58.5 GHz. A very good agreement between simulated and measured MMIC gain and noise performance is achieved up to V-band.**

I. Introduction

MONOLITHICALLY integrated millimeter-wave circuits in the frequency region above 40 GHz are reaching production state for various applications including inter-satellite communications, environmental survey systems, and various radar applications, e.g., collision avoidance radar. A key system component of front end receivers is the low noise amplifier, which has been the focus of our activities. For volume production with high yield and predictable circuit performance, however, a reproducible IC-technology is required in conjunction with accurate CAE models for the active and passive circuit components.

II. Transistor Modeling

Our circuit design approach comprises accurate on-wafer S-parameter characterization and modeling of all circuit components up to 63 GHz. The active devices are PM-MODFETs (Indium mole fraction 25%) on GaAs substrate which have demonstrated at 0.2 μm gate length transit frequencies of 120 GHz [2], [3]. At millimeter-wave frequencies, physically relevant and scalable transistor models are needed to predict the performance of the MMIC correctly. An important issue is the modeling of the parasitic capacitances of the FETs, which have greater effect at millimeter-wave frequencies where the gate length ($Lg \leq 0.3$ μm) and the gate width ($Wg \leq 100$ μm) of the FET have to be reduced. The total parasitic FET capacitances (C_{gsp}, C_{gdp}, C_{dsp}) can be separated into a component which is independent of gate width due to the pad configuration ($C_{gs,pad}$, $C_{gd,pad}$, $C_{ds,pad}$), and a scaling component ($C_{gs,fri}$, $C_{gd,fri}$, $C_{ds,fri}$) which can be associated to the fringing fields in the gate region of the transistor. The accurate determination and location of these components in the topology of the equivalent circuit are therefore an important requirement.

In order to study the parasitic FET capacitances as a function of transistor geometry and layout in detail, passive FET test structures were designed and fabricated on isolated semiconductor material. To allow for the determination of the pad capacitances by extrapolation of the results to zero gate width, four transistor widths were used (50, 100, 150, 200 μm). The passive FETs are realized with 0.25 μm and 0.5 μm gate length, and without gate electrode. In addition, two different layout types were investigated, which will be referred to as a T-layout or U-layout, respectively, according to the arrangement of the gates (Fig. 1).

To determine the parasitic capacitances of the FET structure, the equivalent π-circuit was calculated from the measured S-parameters at each measurement frequency. Due to the high measurement accuracy of on-wafer measurements [4], the capacitance values were consistent within 1 fF in the entire frequency range. Fig. 2 shows the extracted data as a function of gate width for the two different layout types and a gate length of 0.25 μm and 0.5 μm, respectively.

For the three capacitive components C_{gsp}, C_{gdp}, C_{dsp}, there is a linear dependence on gate width. The gated structures extrapolated to zero gate width give the same values for C_{gsp} and C_{gdp} as the structures without a gate electrode with an agreement of better than 1 fF. The scal-

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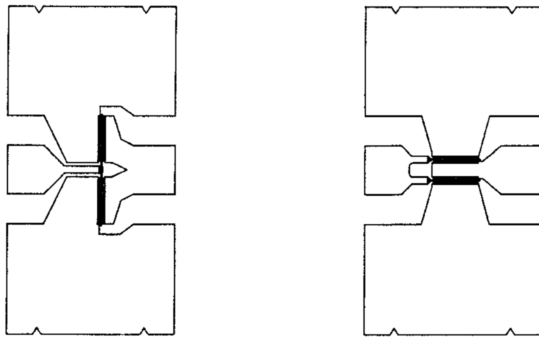


Fig. 1. Millimeter-wave MODFETs in T- and U-layout.

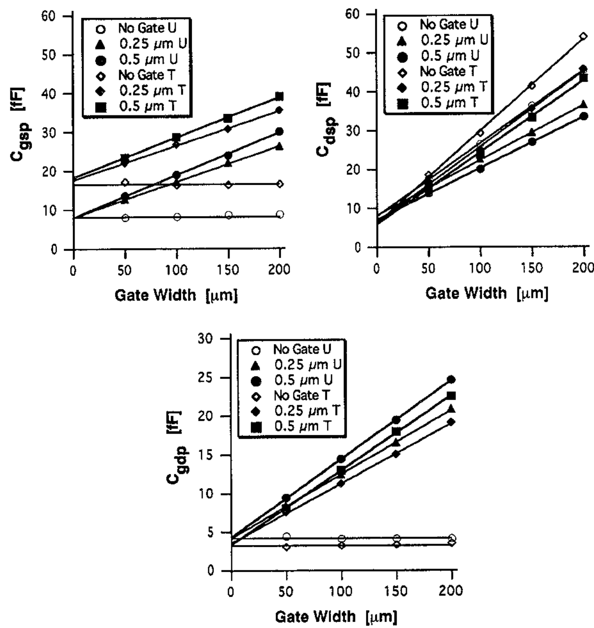


Fig. 2. Parasitic capacitances of passive transistor structures for the two layout types.

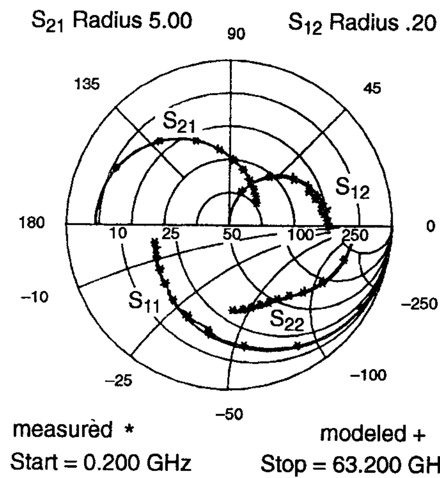


Fig. 3. Measured and calculated S-parameters of a 0.3 μm × 100 μm PM-MODFET in the frequency range from 0.2 GHz and 63.2 GHz.

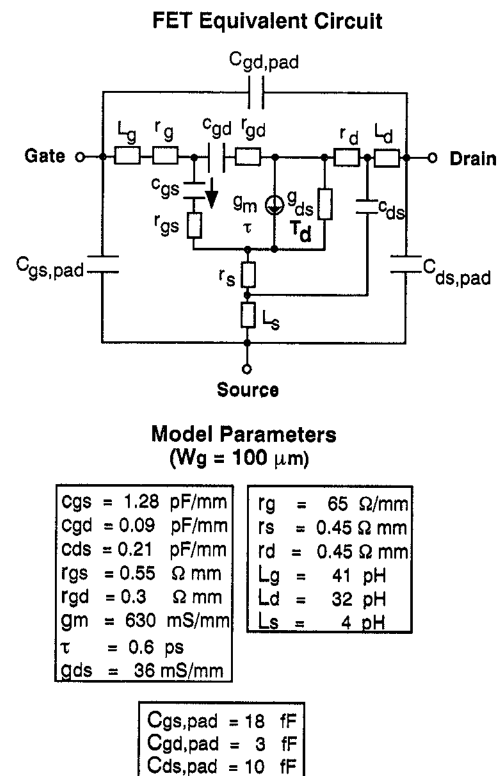


Fig. 4. Equivalent circuit used for S-parameter and noise modeling of MODFETs.

ing component of the structures with the gate is therefore associated with the fringing fields of the gate electrode. In contrast, the parameter C_{dsp} scales with width for both structures and can be associated with fringing fields between the source and drain electrodes. The screening of these fields by the gate electrode accounts for the lower values of C_{dsp} of the gated structures. Comparing the two layout types, the T-layout exhibits a higher $C_{gs,pad}$ than the U-layout because of the longer feed line, whereas the U-layout shows a slightly higher $C_{gd,pad}$ (about 1 fF). The parasitic inductances of the FETs were extracted in the same way from test structures where the gate was short-circuited to the source and drain electrodes.

Using this database, a very good agreement between measured and modeled S-parameters of the active transistor is achieved up to 63 GHz, as can be seen in Fig. 3 for a device with 0.3 μm × 100 μm gate geometry. This shows clearly, that a transistor of this gate width can be modeled very accurately by the lumped element circuit model which is shown in Fig. 4. As a consequence, there is no need for a more complicated model topology, or the use of distributed elements. Model verification was performed by checking the scaling rules of the intrinsic FET for devices with different gate widths. For the 50 μm wide device, the normalized intrinsic elements were within 3% compared to the values given in Fig. 4.

To predict the noise performance of the transistors at millimeter-wave frequencies, we have employed a transistor temperature noise model which is based on the method proposed in [1]. With the temperature model, the noise parameters of the FET can be determined from the circuit model by assigning an equivalent noise temperature to each resistive model element. The calculations

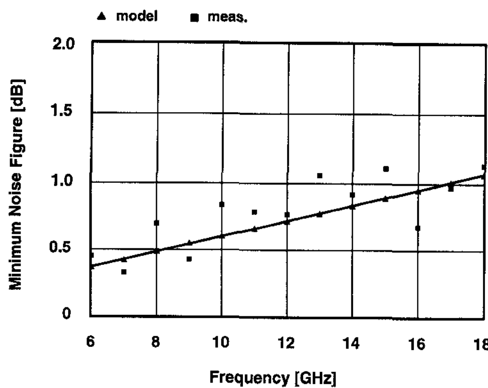


Fig. 5. Minimum noise figure of a 0.3 μm × 100 μm pseudomorphic MODFET, measured and calculated with the temperature model.

were done assigning ambient temperature to all resistors with the exception of the channel resistance r_{ds}, which has a higher noise temperature T_d. This is in accordance to the results for different device temperatures given in [1], which indicate that the FET input noise is thermal. Because of its very small value, the resistor r_{gd} has negligible influence on the noise behavior of the device. For our PM-MODFETs, a temperature of T_d = 1980 K was extracted at low noise bias. Our investigations show, that direct extraction of T_d from measured noise figure can be performed with an uncertainty of 109 K [5].

After the physically relevant and scalable equivalent circuit model of the transistor is derived, the noise parameters of the transistor are measured on-wafer up to 18 GHz. The model output temperature T_d, which is the only remaining parameter needed for the noise model, is extracted by fitting the noise parameters calculated from the equivalent circuit to the measured data. For the MMIC design, the FET temperature noise model was implemented in the commercial Eesof software. A comparison between the calculated and measured minimum noise figure of a 0.3 μm × 100 μm PM-MODFET is given in Fig. 5. The device has a minimum noise figure of 0.7 dB at 12 GHz. Using this noise model, a minimum noise figure of 2.8 dB is calculated at 58 GHz.

III. Modeling of CPW-Structures

We have chosen coplanar waveguide technology because of the advantages regarding technological issues (no substrate thinning or via hole technology required) and circuit performance (grounding of components without additional parasitics, lower transmission line dispersion). In contrast to microstrip structures, there is only a limited database for coplanar MMIC-components, especially in the commercial CAE-tools. To build up an accurate component library which is valid up to millimeter-wave frequencies, a mask set with more than 100 different passive test structures was designed and processed. All circuit relevant CPW-structures, e.g., homogeneous transmission lines, in-line series overlay capacitors, T-junctions, and bias subcircuits, were separately characterized up to 60 GHz. The model parameters of the components were extracted from this data using both analytical and optimization based methods.

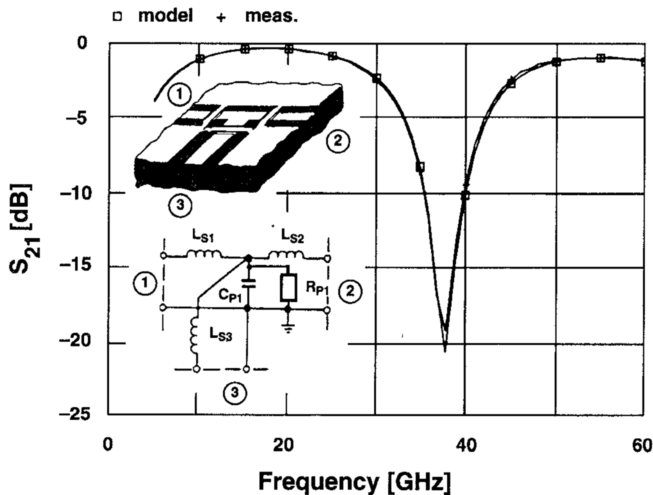
We have recently investigated the influence of the finite metallization thickness on transmission line parameters [7]. For millimeter-wave applications, frequency dispersion phenomena with respect to the effective dielectric constant and the characteristic impedance have to be taken into account. Coplanar lines exhibit a decreasing effective dielectric constant $\epsilon_{r,\mathrm{eff}}$ with increasing frequency, in contrast to conventional microstrip structures. The frequency dispersion of the propagation constant for CPWs, however, is substantially lower compared to microstrip transmission lines [8]. For the CPW transmission lines in the LNAs, a ground-to-ground spacing d = 50 μm was used. The total metalization thickness (first and second metal) is t = 2.7 μm. In Table I, the transmission line parameters at 60 GHz are given for three different CPW lines which are used in the MMICs. It can be noted that the effective dielectric constant $\epsilon_{r,\mathrm{eff}}$ is more than 10% lower compared to the theoretical value ($\epsilon_{r,\mathrm{eff}}$ = 6.95) for zero metalization thickness. The characteristic impedance of the lines is also lower than the value for the ideal case (t → 0, f → 0). The measured values are compared to theoretical values which were calculated from an equivalent circuit model [9] which is based on rigorous field-theoretical results [8]. The measured and calculated data are in very good agreement within the measurement accuracy.

An important building block of our MMIC amplifiers is the coplanar T-junction. We have used a simple 5-element equivalent circuit model as given in Fig. 6 to model the discontinuity. The equivalent circuit topology is chosen in accordance to the related microstrip model [10]. The reactive components L_{S1}, L_{S2}, L_{S3} and C_{P1} of the model represent the perturbations of the electric and magnetic field lines in the conductor strip and the ground planes. To predict the measured S-parameters of the coplanar T-junction correctly, a frequency dependent resistor was added in parallel to the capacitor C_{P1} in order to account for additional loss in the structure (about 0.3 dB at 60 GHz). The additional attenuation may be attributed to radiation losses of the discontinuity which is known for microstrip T-junctions [11].

The elements of the discontinuity model were determined by fitting the model to the measured S-parameters. To check the consistency of the extracted parameters, we have investigated 6 versions of the T-junction with different port 3 termination. This port was connected to short- and open-circuited CPW-lines of three different lengths. The agreement with respect to the extracted model elements was better than 0.5 pH for the series inductances and 1.2 fF for the parallel capacitance. The modeled and measured S-parameters of a coplanar T-junction with a shorted stub of 633 μm length connected at the third port (characteristic impedance of all lines is 50 Ω) are shown in Fig. 6 indicating very good agreement.

TABLE I
CPW LINE PARAMETERS AT 60 GHz FOR THREE DIFFERENT GEOMETRIES

w/d	w μm	Z_0 ideal (t → 0) [Ω]	Z_0 calc. Ref. [9] [Ω]	Z_0 meas. [Ω]	α calc. Ref. [9] [dB/mm]	α meas. [dB/mm]	$\epsilon_{r\,eff}$ calc. Ref. [9]	$\epsilon_{r\,eff}$ meas.
0.75	37.5	33.8	30.8	32.0	0.64	0.65	6.15	6.0
0.40	20.0	51.4	47.9	49.0	0.42	0.45	6.3	6 2
0.18	9.0	70.4	64.9	65.5	0.45	0.45	6.2	6.2



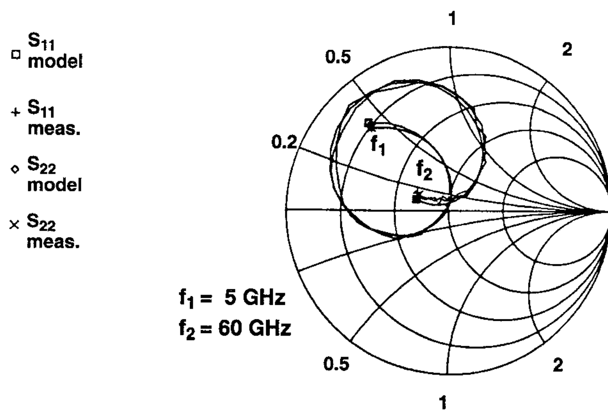


Fig. 6. Measured and modeled two port S-parameters of a CPW T-junction. Port 3 is terminated by a short-circuited transmission line.

IV. CIRCUIT DESIGN

For the verification of our active and passive millimeter-wave component models and basic circuit design concepts, simple single stage MMIC amplifier circuits have been designed in the 40 to 60 GHz region. We have reported results on these single stage MODFET amplifiers recently, which delivered a gain of 9.5 dB, 7.0 dB and 5.0 dB at 40 GHz, 50 GHz, and 60 GHz, respectively [6].

Based on these results, fully integrated 2-stage amplifier MMICs were designed. A band pass design with reactive matching using transmission lines was used. The MMICs include all matching networks and bias subcircuits. The gate geometry of the transistors in the amplifiers is 0.3 μm × 80 μm. The interstage matching network was designed to give a direct impedance transformation between the stages instead of transforming to an impedance of 50 Ω. For the input, output, and interstage matching networks, the unit cells with identical topology were used which comprise three CPW lines connected to a T-junction, a series MIM-capacitor and a bias network. The circuit topology o the LNA is depicted in Fig. 7.

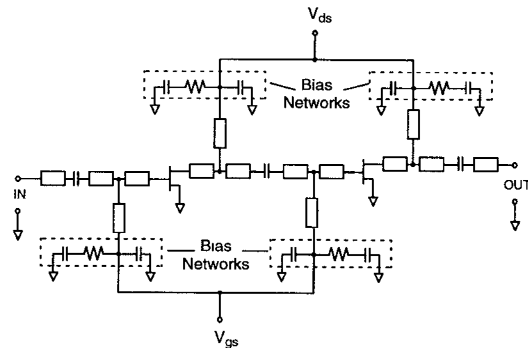


Fig. 7. Circuit topology of the 2-stage LNA.

An important design focus was the stability of the amplifiers, because previous investigations had shown that the amplifiers could tend to oscillate at frequencies between 20 GHz and 30 GHz. Therefore, stability criteria were included in the optimization routine using the CAE tool. As a result of this approach, the realized amplifier circuits were unconditionally stable with a stability factor $k > 1.5$ over the entire frequency region.

V. MILLIMETER-WAVE MEASUREMENT SYSTEMS

Characterization of the passive MMIC-components, MODFETs and LNAs was done using an on-wafer S-parameter measurement system which is based on a HP 8510C network analyzer system extended by a mm-wave test to 63 GHz. The signals of the two test sets are combined using coaxial power combiners. The probe heads are 65 GHz probes with 100 μm pitch size from CASCADE Microtech. During the measurement sequence, the data in the two frequency bands is automatically acquired and combined using our in-house software. The network analyzer was calibrated with the LRM calibration method.

To make accurate noise figure measurements possible at V-band frequencies, we have developed an on-wafer noise measurement system in the 55 to 60 GHz range. In order to achieve high measurement accuracy, the ENR of

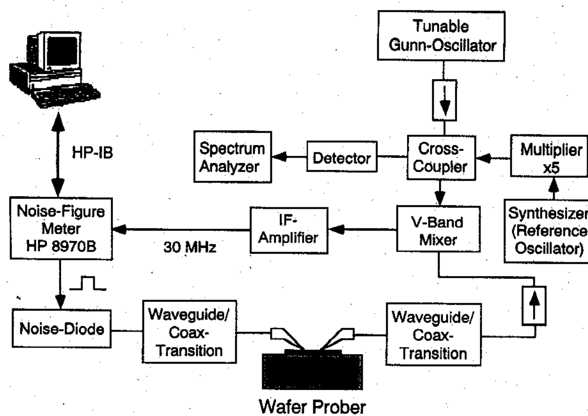


Fig. 8. Block diagram of the millimeter-wave noise filter measurement set up.

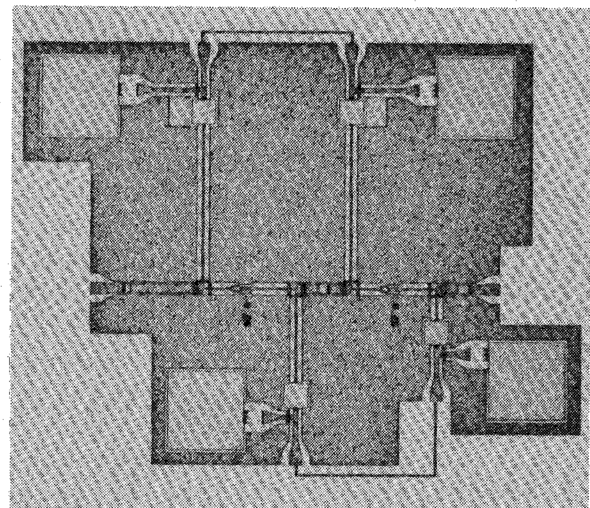


Fig. 9. Micrograph of the 2-stage LNA chip.

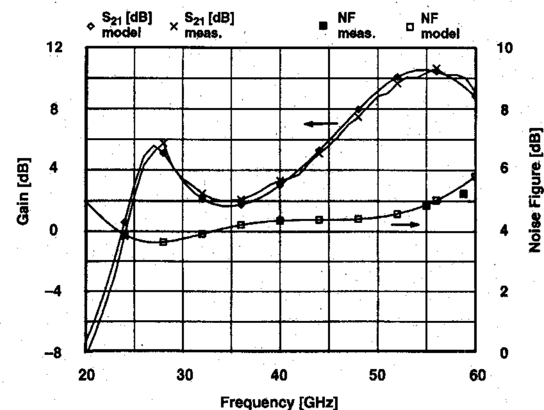


Fig. 10. Gain and noise performance of the 2-stage V-band LNA.

the noise diode at the waveguide reference plane was determined by a hot/cold measurement of a waveguide load at 300 K and 77 K, respectively. Furthermore, the S-parameters of the waveguide/coaxial-transition and wafer probe head were measured. Using this data, the ENR at the coplanar reference plane of the probe tips was calculated. An HP 8970B noise figure meter was used in the measurement system. Fig. 8 shows the block diagram of the millimeter-wave on-wafer noise measurement set up.

VI. MMIC Characterization

The MMICs were fabricated including airbridges, MIM-capacitors and NiCr-resistors. The gate recess of the transistors is performed using a dry etching process with etch stop, which yields a highly constant gate-to-channel separation and therefore good uniformity of the FET parameters across the wafer [2]. The standard deviation of f_T and $f_{\max}$ determined by RF wafer mapping on a 2-inch wafer is typically 1.1% and 1.8%, respectively. Pattern definition is performed using a 'mix and match' e-beam/optical lithography.

A micrograph of the LNA chip is shown in Fig. 9. The chip size of the amplifier is 2.2×1.8 mm^2. The bias pads are configured compatible to the CASCADE microwave probe-heads to facilitate automatic measurements. The measured and calculated gain and noise figure of the MMIC is shown in Fig. 10. The measured gain is better than 10 dB between 55 GHz and 59 GHz. The measured noise figure is 4.8 dB at 55 GHz, and 5.2 dB at 58.5 GHz. Input and output return loss are better than 10 dB in the frequency range from 55 GHz and 60 GHz. Isolation of the amplifier is better than -32 dB in the entire measurement frequency range.

The LNAs were biased at a drain voltage of 3.3 V and a drain current of 190 mA/mm. At this bias condition, the devices have an f_T and $f_{\max}$ of 65 GHz and 130 GHz, respectively. No additional tuning elements, e.g., open stubs were used to achieve the reported performance.

VII. Conclusion

We have developed an accurate CAE database for active and passive MMIC components. The investigated CPW-structures include all relevant MMIC components, e.g., homogeneous transmission lines, in-line series overlay capacitors, T-junctions, and bias subcircuits. The models were verified by on-wafer S-parameter measurements up to 63 GHz. The measured transmission line parameters of homogeneous CPW transmission lines at 60 GHz were found to be in good agreement to field-theory based calculations. For noise modeling of the MODFETs up to millimeter-waves, a novel approach was utilized based on the temperature model.

Using these results, a V-band LNA was designed which has a state-of-the-art performance showing a gain of 10.5 dB and a noise figure of 5.2 dB at 58.5 GHz, in close agreement with predicted results. For noise figure measurements of the LNAs at V-band, an on-wafer noise measurement system was established. The amplifier performance compares favorably to previous results of microstrip LNA with PM-MODFETs of comparable gate length published in [12], [13]. Due to the moderate gate length of 0.3 μm and the reproducible technology process, we

have achieved a high RF circuit yield (80% of the MMICs had more than 8 dB gain at 55 GHz), which is a prerequisite for cost-effective MMIC production.

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